3. OGP120 Design of Ultra Low-Power FHSS Transceiver for Wireless Communication Applications

S.No.	Particulars	Details			
1.	**Project Team**	**PI: Shri Anukul C. Baishya** 	**Co-PI: Shri P P Sahu** 	**Presenter : Shri CH V Narasimha Rao, SFP** 	
2.	**Contact Details**	**Organization/ Institute: Tezpur University** M:9435081172 Email: anukul@tezu.ernet.in	**Organization/ Institute: Tezpur University** Email: pps@tezu.ernet.in Date of Joining of JRF(s): 27.10.2014 and 18.11.2014 (Left the project before completion)		
3.	**SAC Focal Person(s)**	**Shri CH V Narasimha Rao, 5272/ 94**			
4.	**Project Duration**	**Start Date: 25-09-2014**	**Actual Completion Date: 31/03/2018**	**Duration: 2 Years**	
5.	**Budget (with yearly break-up):**	**Year**	**Approved Budget**	**Received Budget**	**Date when Budget received**
		1st Year	29,00,000.00	20,25,000.00	25.9.2014
		2nd Year		2,24,000.00	6.2.2018
		Total Fund	29,00,000.00	22,49,000.00	
6.	**Source of getting information about RESPOND.**	Tick the appropriate: **Through other academic institutions**			
7.	**Salient Features of the Project:** This project is specifically focused on the design and analysis of frequency hopping spread spectrum transceiver for wireless communication applications with particular attention to transmitter and receiver system design. This work also attempts to address the issues associated with the design of some of the critical CMOS RF analog circuits employed in the proposed architecture. The key analog circuit block in the transmitter is the Voltage Controlled Oscillator (VCO) with reasonably wide bandwidth. We have designed a new CMOS current starved voltage controlled ring oscillator (CSVCRO) and verified it by simulating in 0:18µm CMOS technology. The VCO architecture proposed here provides high linear relationship between oscillation frequency over a reasonably lower range of control voltage and results in a large tuning range. The linear frequency sweep is obtained without employing any additional compensation techniques resulting in less circuit complexity, die area and power consumption. We have also custom-designed the digital and mixed signal circuits such as 4-bit data word generator, PN sequence generator, 8:1 multiplexer, serial-to-parallel (S2P) converter, Digital-to-analog converter (DAC)etc. using the standard architectures in order to complete the transmitter system. The key analog circuit blocks in the receiver section are the RF front-ends such as Low noise amplifier (LNA), wide band or frequency independent precision rectifier and the Frequency-to-voltage converter (FVC). We have designed a CMOS based low noise amplifier with L-type input matching network and π- type output matching network. The input L-type matching network is used to fix the Q-factor whereas the output π –type matching network provides an extra degree of freedom to adjust the bandwidth. We have also conceptualized a new sinusoidal full wave precision rectifier				

	architecture which was implemented with 0:18µm CMOS technology. The circuit gives a d.c. output voltage, the magnitude of which is nearly the same as the peak input voltage over a frequency with a very low ripple voltage and low harmonic distortion. We have also designed and implemented the sub-circuits like analog-to-digital converter (ADC), parallel-to-serial converter (P2S), Differentiator, Integrator, Logarithmic and anti-logarithmic amplifiers, Comparator, Coding network etc. in order to complete the receiver system.

8. Technological Experience gained:

S.No.	Planned Objectives	Achieved Objectives	Experience gained
1	Literature survey	completed	Gained experience in state-of-the-art CMOS RF design using low power CMOS technology in wireless communication
2	Transceiver conceptualisation	completed	Learnt about various transceiver systems which helped in conceptualization of the proposed system
3	Transmitter design	completed	Learnt to design the analog and digital circuits using low power CMOS technology
4	Receiver design	completed	Learnt to design the analog and digital circuits using low power CMOS technology
5	System Integration	Partially completed	Learnt to integrate the sub-circuits of both the transmitter and receiver. This is the most time consuming job which needs re-design of many sub-circuits.
6	EDA Tool	completed	Learnt a lot on how to use EDA tool for designing Low power RF circuits using CMOS technology.

9. Details of project deliverable and whether the same is used further?

Deliverables	*Further usages (by ISRO as well as your institute/ other user agencies)*
Hardware	i) FHSS Transceiver system using 0.18 µm CMOS technology in the 2-4 GHz frequency band. ii) Sub-modules of the transceiver system in 0.18 µm CMOS technology

10. Have you been able to improve any hardware/ software/ other deliverable of the project after completion? (through further research) No, because license of the EDA tool is expired and it is too costly.

11. Do you think that the deliverables are used effectively? Share your opinion and reason for your opinion.
Yes, because circuits were designed using the recommended EDA tool and CMOS PDK.

12. How do you rate the deliverable of project? Very Good

13. Is this your first RESPOND Project with SAC? Yes

14. If no, mention details of your earlier project/s with RESPOND : -

15. Human Resource Development at Institute:

Researchers	*Numbers*	*Qualification*
PI	1	Ph.D
Co-PI	1	Ph.D
Other (Specify)	2	M.Tech

16. Whether any researcher has been able to pursue study through project? No

17. If yes, mention type of degree and details. --

<table>
<tr><td rowspan="2">18.</td><td rowspan="2">What is the current profile of JRF/others researchers involved in the project?</td><td>Profile</td><td>Organization</td></tr>
<tr><td>Not Known (Left the project before completion)</td><td>Not Known</td></tr>
<tr><td>19.</td><td colspan="3">Numbers of publications resulted out of the project work, include even those published after project was completed : -</td></tr>
<tr><td>20.</td><td colspan="3">List of Paper Publications : International Journal: To be published</td></tr>
<tr><td>21.</td><td colspan="3">IPR/ MoU: Patent/ Technology Transfer/ MoU (Applied, Granted) No</td></tr>
<tr><td>22.</td><td colspan="3">Awards and Recognition for the Project : -</td></tr>
<tr><td>23.</td><td colspan="3">Whether any workshop/ symposium organized through project? (Both Jointly or Individually) : -</td></tr>
<tr><td rowspan="4">24.</td><td rowspan="4">Details of new/ augmented infrastructure/ facility build through the projects and whether it is in use at present?</td><td>Particulars</td><td>Numbers</td><td>Currently in use as well as purpose (Occasionally, Frequently)</td></tr>
<tr><td>Desktop</td><td>3</td><td>Frequently</td></tr>
<tr><td>Printer</td><td>1</td><td>Frequently</td></tr>
<tr><td>Lab facility</td><td>1</td><td>Frequently</td></tr>
<tr><td>25.</td><td colspan="3">Do you think that the equipments/ facilities / lab/ software/ hardware established through project are useful for the institute? Share your opinion and reason for your opinion. :
Yes, because students are using the facilities for their Project work</td></tr>
<tr><td>26.</td><td colspan="3">Has the project generated any new area or avenue for further research? :
Yes on Low power CMOS VLSI Design</td></tr>
<tr><td>27.</td><td colspan="3">Has the project received any recognition/ award/ appreciation at academic forum? : No</td></tr>
<tr><td>28.</td><td colspan="3">Has the project helped you in your annual appraisal ratings at your institute? : No</td></tr>
<tr><td rowspan="2">29.</td><td rowspan="2">Do you think that RESPOND projects are helping academia in general?</td><td>Particular</td><td>Reason</td></tr>
<tr><td>Yes</td><td>PI s can continue their research by procuring facilities out of project fund which are otherwise not available in the Institutes</td></tr>
<tr><td>30.</td><td colspan="3">According to you, how RESPOND projects can be of more usefulness to academia?:
Already useful</td></tr>
<tr><td>31.</td><td colspan="3">Any other Information/ Suggestion: JRFs left the project around well before completion of the project.</td></tr>
</table>

Observation/ Recommendation:

- Shri CH V Narasimha Rao, SFP, presented the status.
- The project has fulfilled its objectives and very good work has been done. FHSS transceiver has been developed using 180 nm SCL foundry. The same has been tested and delivered to SAC.
- Project is completed during 2018-19. Summary of findings sent to ISRO-HQ.

FORM OF FUND UTILISATION CERTIFICATE

(PROJECTS/SCHEMES)

(2017-2018)

Name of the Nodal Institution : Tezpur University

Department of Organisation : Electronics & Communication Engg

Name of the Project Scheme : RESPOND

Certified that out of Rs 2,24,000.00 of Grant-in-aid sanctioned during the financial year 2017-18 in favour of Anukul C Baishya On the subject project/scheme for the third (first/ second / third) year by Government of India, Department of Space, Bangalore as per Sanction Order No. DOS/PAO/GIA/2017-18/131 dated 06.02.2018 and Rs 1,32,817.00 Unspent balance of the previous year a sum of Rs 2,30,730.00 has been utilized during the current financial year 2017-18 on the Project / Scheme and the balance amount of Rs 1,26,087.00 remaining unutilized at the end of the year will be surrendered to Pay and Accounts Officer, Department of Space, Bangalore duly supported by consolidated Audited statement of accounts, reports, papers, compendium of data analysis etc.

Project Investigator

Head of Institution

(with seal)

Registrar
Tezpur University
Napaam, Tezpur

Registrar

26/10/18

Finance Officer

(with seal)

Joint Registrar
Tezpur University

Auditor

SHEKHAR AGARWAL & ASSOCIATES
TEZPUR, ASSAM
Chartered Accountants

(with seal)

AUDITED STATEMENT OF ACCOUNTS

1. Project Title : "Design of Ultra Low Power FHSS Transceiver for Wireless Communication Applications"
2. Name of the PI & Designation : Anukul C. Baishya
3. Name & Address of Institution : Tezpur University, Po: Napaam, Tezpur, Assam, Pin:784028
4. ISRO/DOS Letter/Sanction Order No.. & Date : ISRO/RES/3/663/2014-15 dtd. July, 2014 & B.1902/46/2014 dtd. 16.9.2014 & DOS/PAO/GIA/2017-2018/131/649 dtd 06.02.2018
5. Period of Statement : 01.04.2017 to 31.03.2018
6. Total Grants Approved/ Grants for the Year : Rs 29.5 lakhs (2nd yr Grant Rs 2.24 lakhs)
7. University/Institute Sanction No & Date: DOS/PAO/GIA/2014-15/52/398 dtd. 25.09.2014
8. Expenditure Statement for the period : 01.04.2017 to 31.03.2018

Sl No.	Budget Item	Amount Sanctioned by ISRO/DOS/		Expenditure incurred	Balance
		Unspent balance of the previous year	Fund received		
1	Equipment	2459.00	0.00	0.00	2459.00
2	Manpower	10483.00	0.00	0.00	10483.00
3	Consumables & supplies	1,02,643.00	0.00	0.00	1,02,643.00
4	Contingency	29,067.00	0.00	0.00	29,067.00
5	Travel	(-) 30590.00	75,000.00	62,975.00	(-) 18,565.00
6	Overhead	18,755.00	1,49,000.00	1,67,755.00	0.00
	Total	**1,32,817.00**	**2,24,000.00**	**2,30,730.00**	**1,26,087.00**

Project Investigator
Technical Officer
Department of Electronics & Communication Engg.
Tezpur University

Finance Officer
26/10/18
Joint Registrar
Tezpur University

Head of the Institution
Registrar
Tezpur University
Napaam, Tezpur

Auditor
SHEKHAR AGARWAL & ASSOCIATES
M. No. 310479
TEZPUR, ASSAM
Chartered Accountants